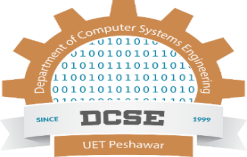
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**University of engineering & technology Peshawar**

**Digital Logic &computer Design-lab**

**Lab report no#05**

**Fall 2020**

**Submitted by: Ashfaq Ahmad**

**Section: B**

**Reg No: 19PWCSE1795**

**Semester: 3rd**

**“On my honor, as a student of University of Engineering and Technology Peshawar, I have neither given nor received unauthorized assistance on this academic work”**

Student signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Submitted to:**

**Eng: Abdullah Hamid**

**Department Of Computer System Engineering**

**OBJECTIVES**

After completing this experiment, you will be able to:

* Design and construct half adder, full adder, half subtractor and full subtractor circuits
* Verify their truth tables using logic gates

**COMPONENTS REQUIRED**

* 7430 or 7408 quad 2-input AND gates
* 7432 quad 2-input OR gates
* 7404 hex inverters
* 7486 quad 2-input XOR gates
* 520 Ω / 1k Ω resistors
* DIP Switch
* LEDs

**THEORY**

A digital adder circuit adds binary signals & a subtractor subtracts binary signals. Half Adder/Subtractor is a basic circuit that adds / subtracts 2 bits and generates Sum or Difference along with Carry / Borrow. Unlike Half Adder or Subtractor a Full Adder / Subtractor has the provision to take consideration of previous Carry / Borrow also.

**Binary Addition Circuits**

Logic gates are used to accomplish the arithmetic operation of binary addition in digital circuits. A two input logic gate is required to accomplish the addition of two binary numbers. The exclusive-OR gate is used to achieve binary addition which is slightly different from basic OR gate.

An inclusive-OR gate or basic OR gate adds integers together and produces an output 1 when both or either inputs are high. However, an OR gate does not achieve the binary addition because of the distinct operation compared with Ex-OR gate.

**Binary subtraction Circuits**

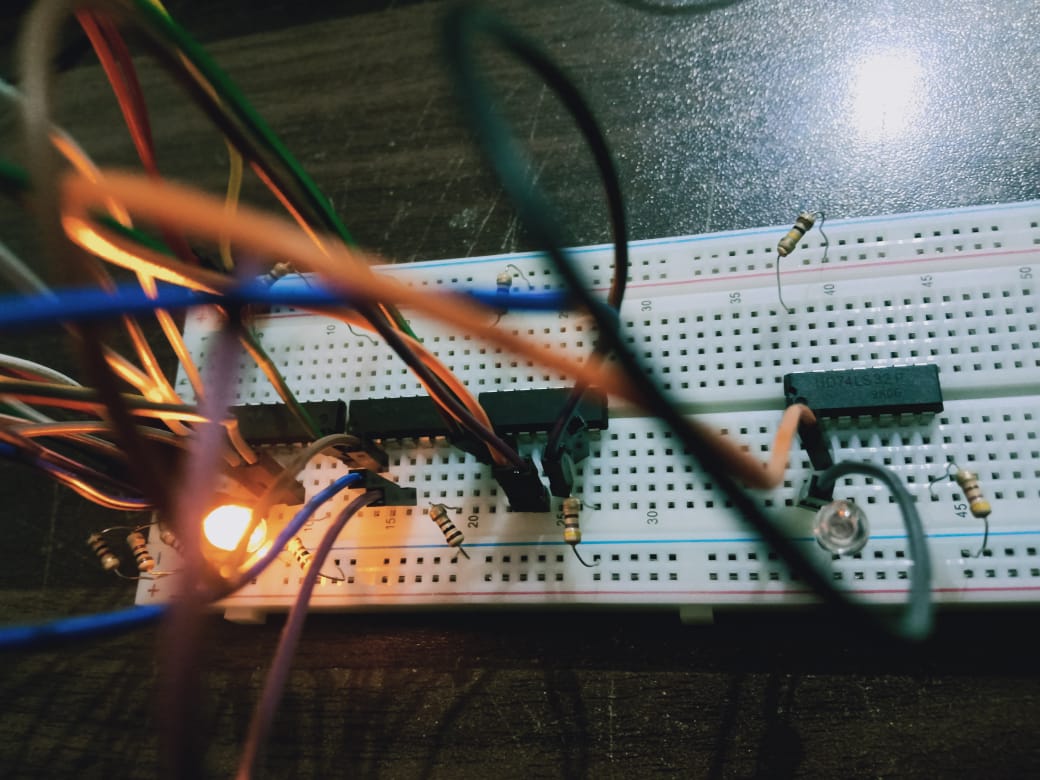
The binary subtraction is also performed by the Ex-OR gate with additional circuitry to perform the borrow operation. Thus, a half subtractor is designed by an Ex-OR gate including AND gate with A input complemented before fed to the gate.

**PROCEEDURE**

* Connections are given as per circuit diagram.
* Logical inputs are given as per circuit diagram.
* Observe the output and verify the truth table.

**Real life picture:**

* Full subtractor using two half subtractor.



**Adder:**

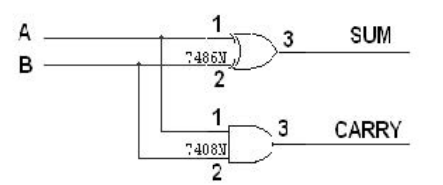
There are two type of adder.

1. **Half adder:**

A logic circuit block used for adding two one bit numbers or simply two bits is called as a half adder circuit. One is called augend and other is called addend. This circuit has two inputs which accept the two bits and two outputs, with one producing sum output and other produce carry output. Half adder has limited number of applications, and practically not used in the application especially multi-digit addition.

To accomplish the binary addition with Ex-OR gate, there is need of additional circuitry to perform the carry operation. Hence, a half adder is formed by connecting AND gate to the input terminals of the Ex-OR gate so as to produce the carry as shown in below figure.

Circuit diagram:



**Truth table:**

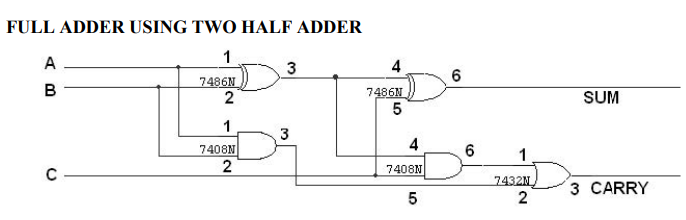
|  |  |  |  |
| --- | --- | --- | --- |
| A | **B** | **carry** | **sum** |
| 0 | **0** | **0** | **0** |
| 0 | **1** | **0** | **1** |
| 1 | **0** | **0** | **1** |
| 1 | **1** | **1** | **0** |

1. **Full adder:**

A binary full adder is a multiple output combinational logic network that performs the arithmetic sum of three input bits. As we have seen that the half adder cannot respond to the three inputs and hence the full adder is used to add three digits at a time.

Full adder can be formed by combining two half adders and an OR gate as shown in above where output and carry-in of the first adder becomes the input to the second half adder that produce the total sum output. The total carry out is produced by ORing the two half adder carry outs as shown in figure. The full adder block diagram and truth table is shown below.

**Circuit diagram:**



**Truth table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | **B** | **C** | **carry** | **sum** |
| 0 | **0** | **0** | **0** | **0** |
| 0 | **0** | **1** | **0** | **1** |
| 0 | **1** | **0** | **0** | **1** |
| 0 | **1** | **1** | **1** | **0** |
| 1 | **0** | **0** | **0** | **1** |
| 1 | **0** | **1** | **1** | **0** |
| 1 | **1** | **0** | **1** | **0** |
| 1 | **1** | **1** | **1** | **1** |

**Subtractor:**

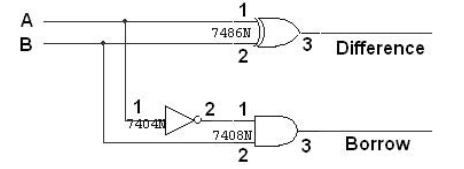
There are two type of subtractor

1. **Half subtractor:**

It has two input variables and two output variables. Two inputs are corresponding to two input bits and two output variables corresponds to the difference bit and borrow bit.

The binary subtraction is also performed by the Ex-OR gate with additional circuitry to perform the borrow operation. Thus, a half subtractor is designed by an Ex-OR gate including AND gate with A input complemented before fed to the gate.

**Circuit diagram:**



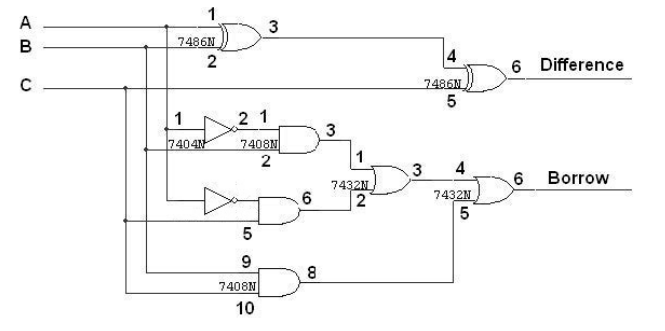
**Truth table:**

|  |  |  |  |
| --- | --- | --- | --- |
| A | **B** | **carry** | **difference** |
| 0 | **0** | **0** | **0** |
| 0 | **1** | **1** | **0** |
| 1 | **0** | **0** | **1** |
| 1 | **1** | **1** | **0** |

1. **Full subtractor:**

It has three input terminals in which two terminals corresponds to the two bits to be subtracted (minuend and subtrahend), and a borrow bit corresponds to the borrow operation. There are two outputs, one corresponds to the difference output and other borrows output Borrow as shown in figure along with truth table.

Circuit diagram:



**Truth table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | **B** | **C** | **carry** | **difference** |
| 0 | **0** | **0** | **0** | **0** |
| 0 | **0** | **1** | **1** | **1** |
| 0 | **1** | **0** | **1** | **1** |
| 0 | **1** | **1** | **1** | **0** |
| 1 | **0** | **0** | **0** | **1** |
| 1 | **0** | **1** | **0** | **0** |
| 1 | **1** | **0** | **0** | **0** |
| 1 | **1** | **1** | **1** | **1** |

**THE END**